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10/798,874	03/10/2004	Glenn F. Evans	3382-67148	6617

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EXAMINER	
AMIN, JWALANT B	
ART UNIT	**PAPER NUMBER**
2628	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,874	EVANS ET AL.	
	Examiner	Art Unit	
	JWALANT AMIN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,35-41,44 and 46-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,35-41,44 and 46-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/28/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/28/2008 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1-4, 35-41, 44 and 46-53 have been considered but are moot in view of the new ground(s) of rejection.

3. Regarding claims 1-4, 35-41, 44 and 46-53, the applicant argues that non of the cited references teach "… assigning zero values to one or more least significant bits in the fractional component while the values and the specific positions of the values of the integer component are unchanged" (see pgs. 10-14).

4. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In this instant case, the examiner interprets that although Eid teaches converting (shifting) the n-bit representation (16 bit integer) to a lower-precision representation (10 bit value) ([0023]), Eid does not explicitly teach that the 16-bit data comprises a most significant byte comprising 8 bits and a least significant byte comprising 8 bits, where the most significant byte forms an integer component and the least significant byte forms a fractional component. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the numbers 'n' and 'k' of an m-bit integer such that 'n' most significant bits would be same as the most significant byte and 'k' least significant bits would be same as the least significant byte so as to make the '8' most significant bits as the integer component and the '8' least significant bits as the fractional component of the 16-bit integer because such a representation could also be used in the systems with 16-bit processors by using both the integer and fractional component of the representation and with 8-bit processors by using just the integer component of the representation.

5. Eid teaches to shift a 16-bit integer by 6 bits to obtain a 10-bit integer ([0023]; shift operation could involve assigning zero values). However, Eid does not explicitly teach that the values and the specific positions of the values of the integer component represented by the most significant byte are unchanged. Denk teaches to convert a real-valued, fixed point two's complement input signal represented by n+a bits in n.a format, to real-valued, fixed point two's complement binary reduced precision output signal represented by n+b bits in n.b format, where a-b bits are designated as the loss portion of the rounding operand ([0082]; Denk teaches to convert from a higher

precision representation to a lower precision representation where the integer component of the signal value, represented by n bits, remains unchanged; it should be noted that the rounding operation will have no effect on the values and specific position of the values of the integer component as the integer component remains unchanged). Therefore, it would have been obvious to one of ordinary skill in the art at the time of present invention to have the integer component comprising n digits remain unchanged as taught by Denk and use it into the method of Eid because the most significant n digits of the higher precision representation n+a constitute the precision portion of the rounding operand, with the remaining a digits being the loss portion ([0057]). Moreover, it would have been obvious to one of ordinary skill in the art at the time of present invention to substitute Eid's known method of shifting with Denk's known method rounding for converting a higher precision representation to a lower precision representation because such a simple substitution of one known method for another would have yielded predictable results to one of ordinary skill in the art.

The combination of Eid and Denk discloses shifting and rounding operations, but they do not explicitly teach to assign zero values to one or more least significant bits in the fractional component without changing the integer component. However, Motorola teaches to use CLR command to clear the destination to all zero (page B-35; using CLR command, the least significant byte, which corresponds to the fractional component of the higher precision representation, could be assigned zero values and converted to the lower precision representation; it should be noted that the limitation of assigning zero values to one or more least significant bits is broad enough to be interpreted as

assigning zero values to the least significant byte; it should be noted that clearing the data and assigning zero values as suggested by Motorola is another method to assign zero values besides shifting and rounding operations). Therefore, it would have been obvious to one of ordinary skill in the art at the time of present invention to substitute the known method of shifting and rounding with the known method of Motorola for converting a higher precision representation to a lower precision representation because such a simple substitution of one known method for another would have yielded predictable results to one of ordinary skill in the art.

6. Regarding claim 1, the applicant further argues "… combining the alleged teaching of Denk with the method of Eid would no longer be shifting as recited in Eid" (see pg. 11).

7. However, the examiner interprets that it would have been obvious to one of ordinary skill in the art at the time of present invention to substitute Eid's known method of shifting with Denk's known method rounding for converting a higher precision representation to a lower precision representation because such a simple substitution of one known method for another would have yielded predictable results to one of ordinary skill in the art.

8. Regarding claim 1, the applicant argues "... Motorola is clearly not operable to clear one or more least significant bits in the fractional component" (see pg. 11).

9. However, the examiner interprets that Motorola teaches to use CLR command to clear the destination to all zero (page B-35; using CLR command, the least significant byte, which corresponds to the fractional component of the higher precision

representation, could be assigned zero values and converted to the lower precision representation; it should be noted that the limitation of assigning zero values to one or more least significant bits is broad enough to be interpreted as assigning zero values to the least significant byte as the least significant byte will have eight least significant bits; it should be noted that clearing the data and assigning zero values as suggested by Motorola is another method to assign zero values besides shifting and rounding operations).

Claim Rejections - 35 USC § 101

10. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

11. Claims 51-53 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

12. Regarding claims 51-53, the computer-readable media, as disclosed in claims 51-53 and described on page 10 of the specification, in the context of this disclosure covers communication medium including carrier waves or other data in a modulated data signal, which are not a Manufacture within the meaning of 101. See MPEP 2106.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1-3, 5, 35, 39-41 and 46-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eid et al. (US 2004/0190771; hereinafter Eid), in view of Denk et al. (US 2001/0025292; hereinafter Denk), and further in view of Motorola's M68000 Programmer's Reference Manual ("M68000 8-/16-/32-Bit Microprocessors: Programmer's Reference Manual", 1986, fifth edition, page B-35, ISBN: 0-13-541491-1, Publication: Prentice-Hall; hereinafter Motorola).

15. Regarding claim 1, Eid teaches a method of converting video data for a video image (motion picture) to a lower-precision representation for lower-precision processing of the video data, the method comprising receiving chroma and luma information for a pixel in the video image in an n-bit representation (representation uses m bits), the n-bit representation comprising a 16-bit fixed-point (this representation uses 16 bits; a fixed point integer color component) block of data per channel ([0012], [0023]; Y(2.14), C(2.14) and alpha(2.14) are all 16 bit fixed-point representation per channel) for the pixel, comprising an integer component (2-bit integer part; n most significant bits) comprising values each with a specific position relative to the 16-bit unit of data (Fig. 1, [0014]; 2-bit integer "XX" corresponds to values each with a specific position relative to the 16-bit unit of data), and a fractional component (14 bit fractional part; k least significant bits) ([0001], [0005], [0006], [0007] last four lines); converting (shifting) the n-bit representation (16 bit integer) to a lower-precision representation (10 bit value) ([0023]), and outputting a result of the converting (fig. 2).

Eid discloses all of the claimed limitations as stated above, but does not explicitly teach that the 16-bit data comprises a most significant byte comprising 8 bits and a least significant byte comprising 8 bits, where the most significant byte forms an integer component and the least significant byte forms a fractional component. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the numbers 'n' and 'k' of an m-bit integer such that 'n' most significant bits would be same as the most significant byte and 'k' least significant bits would be same as the least significant byte so as to make the '8' most significant bits as the integer component and the '8' least significant bits as the fractional component of the 16-bit integer because such a representation could also be used in the systems with 16-bit processors by using both the integer and fractional component of the representation and with 8-bit processors by using just the integer component of the representation.

16. Eid teaches to shift a 16-bit integer by 6 bits to obtain a 10-bit integer ([0023]; shift operation could involve assigning zero values). However, Eid does not explicitly teach that the values and the specific positions of the values of the integer component represented by the most significant byte are unchanged. Denk teaches to convert a real-valued, fixed point two's complement input signal represented by n+a bits in n.a format, to real-valued, fixed point two's complement binary reduced precision output signal represented by n+b bits in n.b format, where a-b bits are designated as the loss portion of the rounding operand ([0082]; Denk teaches to convert from a higher precision representation to a lower precision representation where the integer component of the signal value, represented by n bits, remains unchanged; it should be

noted that the rounding operation will have no effect on the values and specific position of the values of the integer component as the integer component remains unchanged). Therefore, it would have been obvious to one of ordinary skill in the art at the time of present invention to have the integer component comprising n digits remain unchanged as taught by Denk and use it into the method of Eid because the most significant n digits of the higher precision representation n+a constitute the precision portion of the rounding operand, with the remaining a digits being the loss portion ([0057]). Moreover, it would have been obvious to one of ordinary skill in the art at the time of present invention to substitute Eid's known method of shifting with Denk's known method rounding for converting a higher precision representation to a lower precision representation because such a simple substitution of one known method for another would have yielded predictable results to one of ordinary skill in the art.

The combination of Eid and Denk discloses shifting and rounding operations, but they do not explicitly teach to assign zero values to one or more least significant bits in the fractional component without changing the integer component. However, Motorola teaches to use CLR command to clear the destination to all zero (page B-35; using CLR command, the least significant byte, which corresponds to the fractional component of the higher precision representation, could be assigned zero values and converted to the lower precision representation; it should be noted that the limitation of assigning zero values to one or more least significant bits is broad enough to be interpreted as assigning zero values to the least significant byte; it should be noted that clearing the data and assigning zero values as suggested by Motorola is another method to assign

zero values besides shifting and rounding operations). Therefore, it would have been obvious to one of ordinary skill in the art at the time of present invention to substitute the known method of shifting and rounding with the known method of Motorola for converting a higher precision representation to a lower precision representation because such a simple substitution of one known method for another would have yielded predictable results to one of ordinary skill in the art.

17. Regarding claim 2, Eid teaches the n-bit representation is a 16-bit representation and the lower-precision representation is a 10-bit representation ([0023] lines 4-6; 16-bit integer corresponds to n-bit representation; 10-bit value corresponds to lower-precision representation).

18. Regarding claim 3, Eid teaches converting the n-bit representation to an (n-m)-bit representation by assigning zero values to the m least-significant bits in the fractional component [(0023) lines 4-6; 16-bit integer corresponds to n-bit representation; 10-bit value corresponds to (n-m)-bit representation; shifting corresponds to assigning zero values; shifted by 6 bits corresponds to assigning zero values to m least significant bits; the 16-bit ... to obtain a 10-bit value corresponds to converting the n-bit representation to an (n-m)-bit representation by assigning zero values to the m least-significant bits in the least-significant byte). Please refer to the rejection of claim 1 for details regarding assigning zero values to the m least significant bits in the fractional component.

19. Regarding claim 35, Eid teaches the n-bit representation is a 16-bit representation, and the (n-m)-bit representation is a 10-bit representation ([0023] lines

4-6; 16-bit integer corresponds to n-bit representation; 10-bit value corresponds to (n-m)-bit representation).

20. Regarding claim 39, Eid teaches one or more alpha values are associated with the video image ([0001], [0023] lines 6-7; values for alpha components corresponds to one or more alpha values; values for alpha ... 16-bit format corresponds to one or more alpha values are associated with the video image; motion picture data/image data corresponds to video image).

21. Regarding claim 40, Eid teaches a computer system ([0025] lines 1-3; general purpose computer system corresponds to computer system) comprising means for receiving (memory system), means for converting and outputting (microprocessor / multiprocessor computer system) ([0001], [0005] line 4-5, [0028] lines 5-7, [0029] lines 7-11). Please refer to rejection statements of claim 1 for further arguments regarding rejection of claim 40.

22. Regarding claim 41, the statements presented above, with respect to claim 2 and claim 40, are incorporated herein.

23. Regarding claim 46, Eid teaches the computer system further comprising means for displaying the video image using the lower-precision representation ([0025] lines 3-5; output device that displays corresponds to a display).

24. Regarding claim 47, Eid teaches the n-bit representation and the lower-precision representation are most-significant-bit justified ([0020-0023]).

25. Regarding claim 48, Eid teaches the chroma information and the luma information are in a YUV color space ([0001], [0014]; Eid teaches that the components

of a color pixel represents luminance and chrominance). The examiner takes an official notice of the fact that it was known to one of ordinary skill in art that luminance and chrominance of a pixel can be represented in a YUV color space. Therefore, it would have been obvious to one of ordinary skill in art at the time of present invention to use a YUV color space to represent the luminance and chrominance information because video or motion picture data is best stored using YUV color space.

26. Regarding claim 49, the statements presented above, with respect to claim 1 and claim 47, are incorporated herein.

27. Regarding claim 50, the statements presented above, with respect to claim 1 and claim 48, are incorporated herein.

28. Regarding claim 51, Eid teaches a computer-readable medium having computer-executable instructions stored thereon for performing the method of representing video data for a video data image ([0028]; a memory system stores data corresponds to a computer-readable medium having instructions stored; application program corresponds to instructions; an application program to be executed by the microprocessor corresponds to computer-executable instructions). Please refer to the rejection of claim 1 for further details.

29. Regarding claim 52, the statements presented above, with respect to claim 2 and claim 51, are incorporated herein.

30. Regarding claim 53, the statements presented above, with respect to claim 1 and claim 47, are incorporated herein.

31. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eid, Denk and Motorola as applied to claim 1 above, and further in view of Lundberg et al. (US Pub. No.: 2004/0183949; hereinafter referred to as Lundberg).

32. Regarding claim 4, the combination of Eid, Denk and Motorola disclose all of the claimed limitations as stated above, except that they do not explicitly teach that chroma information is sampled at a resolution less than the luma information. However, Lundberg teaches the digital video in YCbCr format is chroma sub-sampled ([0073]; luminance values correspond to luma information; chrominance values/colour information corresponds to chroma information; lower spatial resolution corresponds to at a resolution less than; chroma is sub-sampled ... than the luminance corresponds to the chroma information is sampled at a resolution less than the luma information). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to sample the colour information at lower resolution than the luminance as taught by Lundberg and use such sampling into the method of Eid, Denk and Motorola because human eye is more sensitive to variations in luminance than in chrominance ([0078]).

33. Claims 38 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eid, Denk and Motorola, and further in view of FOURCC.Org - YUV pixel formats (FOURCC.org – YUV pixel formats, http://www.fourcc.orc/yuv.php, pages 1-15; hereinafter referred to as FOURCC.org).

34. Regarding claims 38 and 44, the combination of Eid, Denk and Motorola disclose all of the claimed limitations as stated above, except that they do not explicitly teach that

the n-bit representation and the (n-m)-bit representation are associated with different FOURCC codes. However, FOURCC.org teaches different FOURCC codes for packed YUV formats with different bits per pixel. The labels IYU1 and IYU2 represent 12-bit and 24-bit mode 2 of the IEEE 1934 Digital Camera 1.01 spec format with different FOURCC codes (page 2; IYU2 with 24 bits per pixel corresponds to n-bit representation; IYU2 with 12 bits per pixel corresponds to (n-m)-bit representation/lower-precision representation). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use different FOURCC codes with n-bit representation and (n-m)-bit representation as taught by FOURCC.Org and use it into the method of Eid, Denk and Motorola because using different codes would easily help to identify the different formats used for component representation by looking at the FOURCC codes.

35. Claims 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eid, Denk and Motorola, and further in view of Reitmeier et al. (US Pub. No.: 2003/0202589; hereinafter referred to as Reitmeier).

36. Regarding claims 36 and 37, the combination of Eid, Denk and Motorola disclose all of the claimed limitations as stated above, except that they do not teach that the method comprises processing data in the (n-m)-bit representation using (n-m)-bit hardware, and that the (n-m)-bit representation comprises a 10-bit processor. However, Reitmeier teaches to process 10-bit video signal by coupling it to a video processor ([0033] lines 6-8; 10-bit video signal corresponds to data in the (n-m)-bit representation;

video processor corresponds to hardware; 10-bit video ... to a video processor for further processing corresponds to processing data using (n-m)-bit hardware). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use 10-bit video processor as taught by Reitmeier into the method of Eid, Denk and Motorola because this would help to reduce the cost of processing data by utilizing all the bits available and not wasting any unused bits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JWALANT AMIN whose telephone number is (571)272-2455. The examiner can normally be reached on 10:30 a.m. - 7:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kee M Tung/
Supervisory Patent Examiner, Art Unit 2628

/J. A./
Examiner, Art Unit 2628